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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,164	09/26/2001	Shakuntala Anjanaiah	TI-33533	9586

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
PHAN, MAN U	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,164	ANJANAIAH, SHAKUNTALA	
	Examiner	Art Unit	
	Man Phan	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-14* is/are rejected.

7)☒ Claim(s) *7 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The application of Anjanaiah for the "Apparatus and method for input clock signal detection in an asynchronous transfer mode interface unit" filed 09/26/2001 has been examined. This application claims Priority from Provisional Application 60237237 filed 10/02/2000. Claims 1-15 are pending in the application.

Specification

2. The disclosure is objected to because of the following informalities:

The status of the related application USSN# noted on page 1, lines 10-25 need to be updated.

Appropriate correction is required.

Claim Objections

3. Claim 1, line 6: "a interface reset signal" should be "an interface reset signal"

Claim 2 recites the limitation "a external clock signal" in line 2. This should be "the external clock signal", because it is preceded by the same limitation in claim 1 line 4.

Claim 12, line 12: "a least one control" should change to --at least one control--

Claim 14, line 2: "uits" should change to --units--

Appropriate correction is required.

Claim Rejections - 35 USC # 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 1 12:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 3 are rejected under 35 U.S.C. 1 12, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Claim 3 recites the limitations "the internal clock signals" in line 2. There is no antecedent basis for this limitation in the claim.

b. Claim 6 recites the limitations "the buffer memory" in line 3 and "the direct memory access unit" in line 5. There is no antecedent basis for this limitation in the claim.

c. Claim 7 recites the limitations "the buffer memory unit" in line 2, 3, 5, 6. It's not clear as to whether it is reciting the input buffer memory unit or the output buffer memory unit within the interface unit.

d. Claim 12 recites the limitation "an external data processing unit" in line 2, and "the external processing system" in lines 7, 11. It's not sure they are the same limitation or not.

e. Claim 12 recites the limitation "a direct memory access unit" in line 2, and "the direct memory interface unit" in line 7. It's not sure they are the same limitation or not.

f. Claim 12 recites the limitation "the external clock signal" in line 13. There is no antecedent basis for this limitation in the claim.

g. Claim 15 recites the limitations "the receive event signal" in line 1 and "the transmit event signal" in line 4. There is no antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC ' 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 6 and 8, 9 and 12, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oskouy (US#5,982,772) in view of Dwork et al. (US#5,938,728).

With respect to claim 1-2, Oskouy (US#5,982,772) discloses in Figs. 2 & 3 block diagrams illustrated a system and method for transferring data cells between processing units using UTOPIA protocol. The Cell Interface block 32 transmits and receives cells to the ATM Cell Interface 40 of the network, driven by clock signals provided by Clock Synthesis Circuit 36. Preferably, the ATM Cell Interface 40, and therefore the Cell Interface block 32, conforms to the Universal Test and Operations Physical Interface for ATM ("UTOPIA") standard, as described by the ATM Forum specification. To conform to the UTOPIA specification, the clock synthesis circuit 36 (*clock detection unit*) provides either a clock signal of 20-25 MHz or 40-50 MHz to enable the Cell Interface block 32 to support an 8-bit stream at 20-25 MHz for 155 Mbps or a 16-bit stream at 40-50 MHz for a 622 Mbps data stream (*the transfer of data*

cells being controlled by an external clock signal) (Col. 4, lines 13 plus and Col. 5, lines 59 plus).

However, Oskouy does not disclose expressly the step of generating an interface reset signal for the interface unit. In the same field of endeavor, Dwork et al. (US#5,938,728) discloses an apparatus and method for selectively controlling clocking and resetting of a network interface, comprising a reset detection circuit configured for generating *a reset signal for the network interface* in response to detecting a power-on condition where the reset detection circuit outputs the reset signal until reception of a network clock detection signal. The apparatus also comprises a network clock detecting circuit configured for generating the network clock detection signal a predetermined interval after detection of the network clock, wherein the network interface is configured for loading the initializing information from a nonvolatile memory in response to the reset signal and the network clock. The reset detection circuit ensures that the reset signal is maintained for the network interface until a predetermined interval after detection of the network clock, ensuring the network interface is maintained in a known reset state until the network clock is available to complete initialization of the network interface. In addition, the reset detection circuit maintains the reset signal until after a predetermined interval, such that intermittent network clock signals during initial power up of the network do not adversely affect the network interface, resulting in a more robust initialization routine (Col. 2, lines 18 plus).

Regarding claims 6 and 12, 14, Oskouy further teaches in Fig. 2 depicts an overall system diagram illustrated the architecture of ATM network interface circuit which facilitate the exchange of data. The interface circuit comprises input/output buffer memory units (28, 30) for

transmit/receive data cells, and the interface input/output units (22, 32) for controlling the transmission of data cells (Col. 2, lines 18 plus and Col. 3, lines 51 plus).

Regarding claims 8-9, they are method claims corresponding to the apparatus claims 1-4, 8 above. Therefore, claims 8-9 are analyzed and rejected as previously discussed with respect to claims 1-4, 8.

One skilled in the art would have recognized the need for facilitating the exchange of data between processing units utilizing UTOPIA protocol, and would have applied Dwork's teaching of the controlling clocking and resetting of a network interface into Oskouy's novel use of an ATM UTOPIA interface unit for interfacing with an external system. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Dwork's apparatus and method for selectively controlling clocking and resetting of a network interface into Oskouy's cell interface block partitioning for segmentation and re assembly engine with the motivation being to provide a method and system for input clock signal detection in ATM interface unit.

8. Claims 3-5 and 10, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oskouy (US#5,982,772) in view of Dwork et al. (US#5,938,728) as applied to the claims above, and further in view of Hakkanen et al. (US#5,663,954).

With respect to claims 3-5 and 13, Oskouy (US#5,982,772) and Dwork et al. (US#5,938,728) disclose the claimed limitations discussed in paragraph 7 above. However, these claims differ from the claims above in that the claims require the feature wherein the counter counting the internal clock signals for generating interface reset signal to the UTOPIA

interface unit. In the same field of endeavor, Hakkanen et al. (US#5,663,954) discloses in Fig. 3 a structure of the frame timing for transferring the data cells between processing units, in which the a counter 22 of the frame timing block receives clock pulses (clk) which increment a count value held by the counter; the stored frame length is compared with the counter value after each clock pulse, and when the counter value equals the stored frame length data, the result of the comparison produces an interrupt signal (frame int) to the microcontroller and a reset signal (clr) which resets the counter (Col. 4, lines 37 plus and Col. 8, lines 40 plus)

Regarding claims 10-11, they are method claims corresponding to the apparatus claims 3-5 and 13 above. Therefore, claims 10-11 are analyzed and rejected as previously discussed with respect to claims 3-5 and 13.

One skilled in the art would have recognized the need for facilitating the exchange of data between processing units utilizing UTOPIA protocol, and would have applied Hakkanen's teaching of the counter in generating interface reset signal, and Dwork's teaching of the controlling clocking and resetting of a network interface into Oskouy's novel use of an ATM UTOPIA interface unit for interfacing with an external system. Therefore, It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to apply Hakkanen's frame timing control of TDMA, and Dwork's apparatus and method for selectively controlling clocking and resetting of a network interface into Oskouy's cell interface block partitioning for segmentation and re assembly engine with the motivation being to provide a method and system for input clock signal detection in ATM interface unit.

Allowable Subject Matter

9. Claims 7 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The closest prior art of record fails to disclose or suggest wherein the receive event signal is generated when the input buffer memory unit has a complete data cell stored therein, the receive event signal being cleared when transfer between the input buffer memory unit and the direct memory access unit is begun, and wherein the transmit event signal is generated when the output buffer memory unit has space for a complete data cell, the transmit event signal being cleared when the transfer of the data cell to the output buffer memory unit from the direct memory access is begun, as specifically recited in claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Oskouy (US#5,600,650) is cited to show the method and apparatus for synthesizing clock signal for use with an ATM system having selectable data transmission rates.

The Oskouy et al. (US#5,625,625) is cited to show the method and apparatus for partitioning data load and unload functions within an interface system for use with an ATM system.

The Miller et al. (US#5,796,735) is cited to show the system and method for transmission rate control in a SAR circuit under ATM protocol.

The Hann et al. (US#6,700,872) is cited to show the method and system for testing a UTOPIA network element

The Hann et al. (US#6,862,294) is cited to show method and apparatus for overcoming large transport delays between master and slave UTOPIA devices.

The Hann et al. (US#6,449,655) is cited to show method and apparatus for communication between network devices operating at different frequencies.

The Kimv (US#5,974,047) is cited to show the method for decouping a cell rate in ATM.

The Eum et al. (US#2003/0021277) is cited to show the physical layer duplicating apparatus and method of ATM exchange.

The Carlsson (US#6,256,308) is cited to show the multi-service circuit for telecommunications.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Phan whose telephone number is (571) 272-3149. The examiner can normally be reached on Mon - Fri from 6:00 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu, can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2600.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at toll free 1-866-217-9197.

Mphan

09/13/2005.

Man U. Phan

MAN U. PHAN
PRIMARY EXAMINER